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1 Energy aware compilation for DSPs with SIMD instructions
Markus Lorenz, Lars Wehmeyer, Thorsten Dräger
June 2002 **ACM SIGPLAN Notices , Proceedings of the joint conferenc compilers and tools for embedded systems: software and cor embedded systems LCTES/SCOPES '02**, Volume 37 Issue 7
Publisher: ACM Press
Full text available: pdf(220.77 KB) Additional Information: full citation, abst citings, index ter

The growing use of digital signal processors (DSPs) in embedded syster use of optimizing compilers supporting special hardware features. In this compiler optimizations with the aim of minimizing energy consumption applications: This comprises loop optimizations for exploitation of SIMI zero overhead hardware loops in order to increase performance and decr consumption. In addition, we use a phase coupled code generator ...

Keywords: DSP, SIMD instruction, energy minimization, vectorization, hardware loop

2 Exploiting SIMD parallelism in DSP and multimedia algorithms using the

Huy Nguyen, Lizy Kurian John
May 1999 **Proceedings of the 13th international conference on Superco**
Publisher: ACM Press
Full text available: pdf(1.16 MB) Additional Information: full citation, refe index terms

3 Simulation and architecture evaluation: Vector vs. superscalar and VLIW a embedded multimedia benchmarks
Christoforos Kozyrakis, David Patterson
November 2002 **Proceedings of the 35th annual ACM/IEEE internatio Microarchitecture MICRO 35**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.34 MB) Publisher Site Additional Information: full citation, abst citings, index ter

Multimedia processing on embedded devices requires an architecture tha performance, low power consumption, reduced design complexity, and s this paper, we use EEMBC, an industrial benchmark suite, to compare th architecture to superscalar and VLIW processors for embedded multime comparison covers the VIRAM instruction set, vectorizing compiler, anc that integrates a vector processor with DRAM main memory.We de ...

4 MOM: a matrix SIMD instruction set architecture for multimedia applicati
Jesus Corbal, Roger Espasa, Mateo Valero
January 1999 **Proceedings of the 1999 ACM/IEEE conference on Super (CDROM) Supercomputing '99**
Publisher: ACM Press
Full text available: pdf(116.12 KB) Additional Information: full citation, refe

5 Register file and memory system design: Three-dimensional memory vecto bandwidth media memory systems
Jesus Corbal, Roger Espasa, Mateo Valero
November 2002 **Proceedings of the 35th annual ACM/IEEE internatio**

Microarchitecture MICRO 35

Publisher: IEEE Computer Society Press

Full text available: pdf(1.29 MB) Publisher Site Additional Information: full citation, abst index terms

Vector processors have good performance, cost and adaptability when ta applications. However, for a significant number of media programs, con configurations fail to deliver enough memory references per cycle to fee functional units. This paper addresses the problem of the memory bandw novel mechanism suitable for 2-dimensional vector architectures and tar high effective bandwidth for SIMD memory instructions. The basi ...

6 MEDEA workshop: Indirect VLIW memory allocation for the ManArray n

Nikos P. Pitsianis, Gerald G. Pechanek

March 2003 **ACM SIGARCH Computer Architecture News**, Volume 3

Publisher: ACM Press

Full text available: pdf(623.03 KB) Additional Information: full citation, abst index terms

The indirect very long instruction word (iVLIW) architecture and its imp BOPS ManArray family of multiprocessor digital signal processors (DSI scalable alternative to the wide instruction busses usually required in a m VLIW DSP. The ManArray processors indirectly access VLIWs from sn VLIWs localized in each processing element. With this work, we presen perform 1) iVLIW instruction memory allocation on multiple processing

7 Array recovery and high-level transformations for DSP applications

Björn Franke, Michael O'boyle

May 2003 **ACM Transactions on Embedded Computing Systems (TEC** 2

Publisher: ACM Press

Full text available: pdf(744.35 KB) Additional Information: full citation, abst citings, index ter

Efficient implementation of DSP applications is critical for many embed Optimizing compilers for application programs, written in C, largely foc generation and scheduling, which, with their growing maturity, are provi returns. As DSP applications typically make extensive use of pointer arit

alternative use of high-level, source-to-source, transformations has been
This article develops an array recovery technique that automatically ...

Keywords: Pointer conversion, dataflow graphs, embedded processors, l
transformations

8 Regular contributions: DSP architectures: past, present and futures
Edwin J. Tan, Wendi B. Heinzelman
June 2003 **ACM SIGARCH Computer Architecture News,** Volume 31
Publisher: ACM Press
Full text available: pdf(1.27 MB) Additional Information: full citation, abst

As far as the future of communication is concerned, we have seen that th
for audio and video data to complement text. Digital signal processing (I
that enables traditionally analog audio and video signals to be processed
transmission, storage, reproduction and manipulation. In this paper, we v
various DSP architectures and its silicon implementation. We will also d
the art and examine the issues pertaining to pe ...

9 Code selection for media processors with SIMD instructions
Rainer Leupers
January 2000 **Proceedings of the conference on Design, automation and**
DATE '00
Publisher: ACM Press
Full text available: pdf(147.30 KB) Publisher Site Additional Information: full citation, refe
index terms

10 Compilers and Optimization: An empirical evaluation of high level transfo
embedded processors
Björn Franke, Michael O'Boyle
November 2001 **Proceedings of the 2001 international conference on C**
architecture, and synthesis for embedded systems CAS
Publisher: ACM Press

Full text available: pdf(499.08 KB) Additional Information: full citation, abst index terms

Efficient implementation of DSP applications are critical for many embe Optimising compilers for application programs written in C, largely focu generation and scheduling which, with their growing maturity, are provi returns. This paper empirically evaluates another approach, namely high source transformations. High level techniques were applied to the DSPst 3 platforms: TriMedia TM-1000, Texas Instruments TMS320C6201 and

11 Evaluating MMX technology using DSP and multimedia applications
Ravi Bhargava, Lizy K. John, Brian L. Evans, Ramesh Radhakrishnan
November 1998 **Proceedings of the 31st annual ACM/IEEE internation Microarchitecture MICRO 31**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.52 MB) Additional Information: full citation, refe index terms

Keywords: MMX, digital signal processing, machine measurement, perf monitoring, workload characterization

12 Exploiting a new level of DLP in multimedia applications
Jesus Corbal, Mateo Valero, Roger Espasa
November 1999 **Proceedings of the 32nd annual ACM/IEEE internatio Microarchitecture MICRO 32**
Publisher: IEEE Computer Society
Full text available: pdf(931.68 KB) Publisher Site Additional Information: full citation, abst citings, index ter

This paper proposes and evaluates MOM: a novel ISA paradigm targetec applications. By fusing conventional vector ISA approaches together wit SIMD-like (Single Instruction Multiple Data) ISAs (such as MMX), we new matrix oriented ISA which efficiently deals with the small matrix st found in multimedia applications. MOM exploits a level of DLP not reac conventional vector ISAs nor SIMD-like media ISA extensi ...

13 HIBRID-SOC: a multi-core architecture for image and video applications
S. Moch, M. Bereković, H. J. Stolberg, L. Friebe, M. B. Kulaczewski, A. D
September 2003 **ACM SIGARCH Computer Architecture News , Proce workshop on MEmory performance: DEaling with Ap and architecture MEDEA '03**, Volume 32 Issue 3
Publisher: ACM Press
Full text available: pdf(245.38 KB) Additional Information: full citation, abst

The HiBRID-SoC multi-core architecture targets a wide range of applica particularly high processing demands, including general signal processin video de-encoding, image processing, or a combination of these tasks. F HiBRID-SoC integrates three fully programmable processor cores and v a single chip, all tied to a 64-Bit AMBA AHB bus. Its memory subsyste adapted to the high bandwidth demands of the multi-core a ...

14 Graph-based code selection techniques for embedded processors
October 2000 **ACM Transactions on Design Automation of Electronic S (TODAES)**, Volume 5 Issue 4
Publisher: ACM Press
Full text available: pdf(356.83 KB) Additional Information: full citation, abst index terms, revi

Code selection is an important task in code generation for programmable the goal is to find an efficient mapping of machine-independent interme processor-specific machine instructions. Traditional approaches to code on tree parsing which enables fast and optimal code selection for interme a set of data-flow trees. While this approach is generally useful in compi purpose processors, it may lead to poor code ...

Keywords: SIMD instructions, code selection, data-flow graphs, embed irregular data paths

15 Compilers I: Affinity-based cluster assignment for unrolled loops
Gayathri Krishnamurthy, Elana D. Granston, Eric J. Stotzer
June 2002 **Proceedings of the 16th international conference on Superco**

Publisher: ACM Press
Full text available: pdf(633.13 KB) Additional Information: full citation, abst citings, index ter

To compete performance-wise, modern VLIW processors must have fast high instruction-level parallelism (ILP). Partitioning resources (function registers) into clusters allows the processor to be clocked faster, but oper clusters can easily become a bottleneck. Increasing the number of functi the potential ILP, but only helps if the functional units can be kept busy. features, optimizations such as loop unrolling m ...

Keywords: VLIW architectures, affinity-based clustering (ABC) algorit assignment, homogeneous clusters, loop optimizations, loop scheduling, partitioned register files, software pipelining

16 Trident: a scalable architecture for scalar, vector, and matrix operations
Mostafa I. Soliman, Stanislav G. Sedukhin
January 2002 **Australian Computer Science Communications , Proceed Asia-Pacific conference on Computer systems architectu** Volume 24 Issue 3
Publisher: Australian Computer Society, Inc., IEEE Computer Society Pre
Full text available: pdf(814.51 KB) Additional Information: full citation, abst citings, index ter

Within a few years it will be possible to integrate a billion transistors on this integration level, we propose using a high level ISA to express paral instead of using a huge transistor budget to dynamically extract it. Since data structures for a wide variety of applications are scalar, vector, and m Trident processor extends the classical vector ISA with matrix operation processor consists of a set of paralle ...

Keywords: data parallelism, parallel processing, ring register file, scalat vector/matrix processing

17 Low power DSP's for wireless communications (embedded tutorial session
Ingrid Verbauwhede, Chris Nicol
August 2000 **Proceedings of the 2000 international symposium on Low**

and design ISLPED '00

Publisher: ACM Press

Full text available: pdf(424.32 KB) Additional Information: full citation, abst citings, index ter

Wireless communications and more specifically, the fast growing penetr phones and cellular infrastructure are the major drivers for the developm programmable Digital Signal Processors (DSPs). In this tutorial, an over of recent developments in DSP processor architectures, that makes them execute computationally intensive algorithms typically found in commu DSP processors have adapted instruction sets, memory archi ...

Keywords: architectures, digital signal processing, programmable proce communications

18 Improving 3D geometry transformations on a simultaneous multithreaded S

Claude Limousin, Julien Sebot, Alexis Vartanian, Nathalie Drach-Temam

June 2001 **Proceedings of the 15th international conference on Superco**

Publisher: ACM Press

Full text available: pdf(219.10 KB) Additional Information: full citation, abst citings, index ter

In this paper we evaluate the performance of an SMT processor used as t processor for a 3D polygonal rendering engine. To evaluate this approac PMesa (a parallel version of Mesa) which parallelizes the geometry stag We show that SMT is suitable for 3D geometry and we characterize the geometry stage in term of memory hierarchy, which is the main bottlene that latency is not fully recovered by SMT; the use of L2 ...

Keywords: SIMD extensions, SMT, applications specific architectures, data prefetching, parallel rendering

19 HiBRID-SoC: A Multi-Core System-on-Chip Architecture for Multimedia Applications

Hans-Joachim Stolberg, Mladen Berekovic, Lars Friebe, Soren Moch, Seba Mao, Mark B. Kulaczewski, Heiko Klusmann, Peter Pirsch

March 2003 **Proceedings of the conference on Design, Automation and**

Designers' Forum - Volume 2 DATE '03

Publisher: IEEE Computer Society

Full text available: pdf(307.90 KB) Additional Information: full citation, abst Publisher Site

The HiBRID-SoC multi-core system-on-chip targets a wide range of app particularly high processing demands, including general signal processin video and audio de-/encoding, and a combination of these tasks. For this HiBRID-SoC integrates three fully programmable processors cores and onto a single chip, all tied to a 64-Bit AMBA AHB bus. The processor c optimized to the particular computational characteristics ...

20 Polygon rendering on a stream architecture

John D. Owens, William J. Dally, Ujval J. Kapasi, Scott Rixner, Peter Mat August 2000 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS Graphics hardware HWWS '00**

Publisher: ACM Press

Full text available: pdf(161.65 KB) Additional Information: full citation, abst citings, index ter

The use of a programmable stream architecture in polygon rendering pro mechanism to address the high performance needs of today's complex sc need for flexibility and programmability in the polygon rendering pipeli a polygon rendering pipeline maps into data streams and kernels that ope how this mapping is used to implement the polgyon rendering pipeline o programmable stream processor. We compare our resul ...

Keywords: OpenGL, SIMD, graphics hardware, kernels, media processc rendering, stream architecture, stream processing, streams

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IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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Franchetti, F.; Puschel, M.;
Parallel and Distributed Processing Symposium., Proceedings Internationa
15-19 April 2002 Page(s):20 - 26
Digital Object Identifier 10.1109/IPDPS.2002.1015494
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2. **A survey of parallel computer architectures**
Duncan, R.;
Computer
Volume 23, Issue 2, Feb. 1990 Page(s):5 - 16
Digital Object Identifier 10.1109/2.44900
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3. **Short vector code generation and adaptation for DSP algorithms**
Franchetti, F.; Puschel, M.;
Acoustics, Speech, and Signal Processing, 2003. Proceedings. (ICASSP '0
Volume 2, 6-10 April 2003 Page(s):II - 537-40 vol.2
Digital Object Identifier 10.1109/ICASSP.2003.1202422
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4. **Architecture independent short vector FFTs**
Franchetti, F.; Karner, H.; Kral, S.; Ueberhuber, C.W.;
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Volume 2, 7-11 May 2001 Page(s):1109 - 1112 vol.2
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5. **OPSILA: a vector and parallel processor**
Boeri, F.; Auguin, M.;
Computers, IEEE Transactions on
Volume 42, Issue 1, Jan. 1993 Page(s):76 - 82
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IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

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1. **Introducing a new cache design into vector computers**
Quing Yang;
Computers, IEEE Transactions on
Volume 42, Issue 12, Dec. 1993 Page(s):1411 - 1424
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